OIPE IAP19
MAR 17 2006
PATENT & TRADEMARK OFFICE

3520-06

AF

DPW

PTO/SB/17 (01-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	10/016,939
Filing Date	December 14, 2001
First Named Inventor	Glen E. Roeters, et al.
Examiner Name	David A. Zarneke
Art Unit	2891
Attorney Docket No.	DPAC-052A / AK 155574

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-3534 Deposit Account Name: Andrews Kurth LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 20 or HP =	_____	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 3 or HP =	_____	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____	(round **up** to a whole number) x	_____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Filing a brief in support of an appeal	$500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 45,428	Telephone 512-320-9236
Name (Print/Type)	J. Roger Williams, Jr.		Date March 17, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Express Mail Label No.: EV760876774US

ANDREWS
ATTORNEYS KURTH LLP

Andrews & Kurth L.L.P.
111 Congress Avenue, Suite 1700
Austin, Texas 78701
512.320.9200 Phone
512.320.9292 Fax
andrewskurth.com

J. Roger Williams, Jr.
512.320.9236 Direct

March 17, 2006

VIA EXPRESS MAIL NO.: EV760897677 4US

MAIL STOP – Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re:	Application No.:	10/016,939
	Title:	CSP Chip Stack With Flex Circuit
	Filing Date:	December 14, 2001
	Docket No.:	DPAC-052A / AK 155574

Dear Commissioner:

Please find enclosed for filing the following:

1. Appeal Brief (15 pages);
2. Fee Transmittal for FY 2006 (with duplicate); and
3. A return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees deemed to be due or credit any overpayment to Deposit Account No. 50-3534, upon which the undersigned is authorized to sign.

Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS KURTH LLP

J. Roger Williams, Jr.
Registration No. 45,428

JRW/at
Enclosures

OIPE IAP19
MAR 17 2006
PATENT & TRADEMARK OFFICE

THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

INVENTORS:	Glen E. Roeters and Andrew C. Ross
APPLICATION NO.:	10/016,939
FILING DATE:	December 14, 2001
TITLE:	CSP Chip Stack with Flex Circuit
EXAMINER:	David A. Zarneke
ART UNIT:	2891

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

The real party in interest hereby appeals from the Examiner's claim rejections in the final Office action mailed October 19, 2005 (the "October Rejection") and, to the extent relevant, the Office action mailed March 9, 2005 (the "March Rejection") (collectively, the "Rejection").

This appeal brief is submitted with respect to a Notice of Appeal under 37 C.F.R. § 1.191 that was filed by Express Mail on March 14, 2006, accompanied by a petition to extend the deadline for responding to the October Rejection and payment of the fee for a 2-month extension.

03/20/2006 YPOLITE1 00000113 503534 10016939
01 FC:1402 500.00 DA

CERTIFICATE OF MAILING UNDER 37 CFR §1.10

"Express Mail" mailing label number: EV760876774US

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service in an envelope addressed to Mail Stop Appeal Briefs-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 17, 2006.

Angela Trampel

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Staktek Group, L.P. ("Staktek"), the assignee of all right, title and interest in the above-referenced application.

II. RELATED APPEALS AND INTERFERENCES

Staktek, and Staktek's legal representatives in this case, do not know of any other prior or pending appeals, interferences, or judicial proceedings that may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-21 are pending in the application. Claims 22-25 were cancelled without prejudice. Claims 10-21 have been withdrawn. Claims 1-9 stand rejected. Claims 1-9 are hereby appealed.

IV. STATUS OF AMENDMENTS

No amendments in this case have been filed, either prior to or subsequent to the October Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is the only independent claim at issue. Claim 1 is directed to a chip stack that includes a flex circuit 12 and at least two integrated circuit chip packages 28 electrically connected to a first conductive pattern comprised within the flex circuit 12 (Fig. 1). The flex circuit 12 comprises a flex substrate 14 (Fig. 2), a first conductive pattern disposed on the flex substrate (Specification,[1] par. 0014; Fig. 2), and a plurality of leads 26 extending from the flex substrate 14 and electrically connected to the first conductive pattern. (Figs. 1, 2).

The flex substrate 14, in disclosed embodiments, is rectangularly configured, with a generally planar top surface 16, generally planar bottom surface 18, and opposed pairs of longitudinal peripheral edge segments 20 and lateral peripheral edge segments 22 (Specification,

[1] References to "Specification" refer to the Specification as filed with the Patent and Trademark Office and the paragraph numbers identified therein. Note that the paragraph numbers in the specification as published (publication no. US 2003/0111736 A1) differ by 2 from the paragraph numbers in the specification as filed. In other words, paragraph 0014 in the Specification as filed is paragraph 0016 in the specification as published.

par. 13; Fig. 2). Flex substrate 14 can also be formed in alternative shapes, such as a square. (Specification, par. 0014).

The first conductive pattern, in disclosed embodiments, has a first set of flex pads 24 on the top surface 16 of flex substrate 14 and a second set of flex pads 25 on the bottom surface 18 of flex substrate 14 (Specification, par. 0014; Figs. 1, 2). Although in one embodiment the flex pads 24 and 25 are arranged in identical generally-rectangular patterns, flex pads 24 and flex pads 25 can alternatively be arranged in dissimilar patterns. (Specification, par. 0014; Fig. 2).

The first conductive pattern includes any number of routing configurations connecting the flex pads to each other and leads 26. For example, each flex pad 24 and 25 could be connected to respective ones of lead 26, two or more flex pads 24 or 25 could be electrically connected to a single lead 26, one or more flex pads 24 could be electrically connected in combination with one or more flex pads 25 to a single lead 26, and any flex pad 24 on the top surface 16 of flex substrate 14 can be electrically connected to a coaxially-aligned flex pad 25 on the bottom surface 18 of flex substrate 14 by a via or feed through hole extending through the flex substrate 14 between the coaxially-aligned flex pads. (Specification, par. 0015). In short, the "**first conductive pattern may include conductive traces which extend within the flex substrate 14 in any pattern or arrangement as is needed to achieve a desired signal routing.**" (Specification, par. 0015) (emphasis supplied).

The conductive traces and flex pads, in the disclosed embodiment, are fabricated from very thin copper, between 5 and 25 microns in thickness, through the use of conventional etching techniques. (Specification, par. 0016). "The use of thin copper for the various pads and traces allows for etching line widths and spacings down to a pitch of about four mils, which substantially increases the routing density of the flex circuit 12." (Specification, par. 0016). "**The flex substrate 14 is preferably fabricated from either FR-4, a polyamide film, or some other suitable material which can easily be routed,**" and "may be as thin as about 50 microns or may be a thicker multi-layer structure." (Specification, par. 0016) (emphasis supplied).

Paragraph 0017 of the specification describes a preferred embodiment of the integrated circuit chip packages 28. Each of the integrated circuit chip packages 28 includes a rectangularly configured package body 30 with generally planar top and bottom surfaces 32 and 34, opposed pairs of longitudinal and lateral sides, and on the bottom surface 34 a plurality of spherically or semi-spherically shaped conductive contacts 36 which can be electrically connected to flex pads

24 and 25. (Specification, par. 0017; Figs. 1, 2). "Each of the integrated circuit chip packages 28 is preferably a CSP (chip scale package) device such as a BGA (ball grid array) device, a fine pitch BGA device, or a flip chip device." (Specification, par. 0017; Fig. 1).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Staktek requests review of the following grounds of rejection asserted by the Examiner in the Rejection:

- Rejection of claims 1-4, 6 and 7 under U.S.C. 102(b) as being anticipated by Watanabe, et al., US Patent 4,982,265 ("Watanabe"); and
- Rejection of claims 5, 8, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe.

VII. ARGUMENT

A. Rejection of Claims 1-4, 6 and 7 Under 35 U.S.C. § 102(b) as Being Anticipated by Watanabe

A claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See e.g.*, MPEP § 2131, *citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Watanabe does not anticipate independent claim 1 because it discloses neither the "flex substrate" nor the "integrated circuit chip packages" limitations of claim 1. Since Watanabe does not anticipate claim 1, Watanabe also does not anticipate claims 2-4, 6, and 7, which depend directly or indirectly from claim 1.

1. Watanabe Does Not Disclose A "Flex Circuit."

The Rejection contends that the "flex substrate" limitation in claim 1 is met by the module base plate 1 taught in figures 1 and 2 of Watanabe. (March Rejection, at p. 3; October Rejection, at pp. 2, 4). According to the Rejection, a ceramic material such as the module base plate 1 meets the limitation of a "flex substrate" because "**all things are flexible, at least to some degree.**" (October Rejection, at p. 4). This ground of rejection is in error because it would comprehend any substrate at all, even if made of the most rigid material known to man. The module base plate 1 taught in figures 1 and 2 of Watanabe does not satisfy the "flex substrate" limitation of claim 1 because nothing in Watanabe teaches or suggests that the module base plate

1 is flexible.

a) The Module Base Plate 1 Taught By Watanabe.

The module base plate 1 of Watanabe is shown in Figures 2 and 3:

FIG. 2

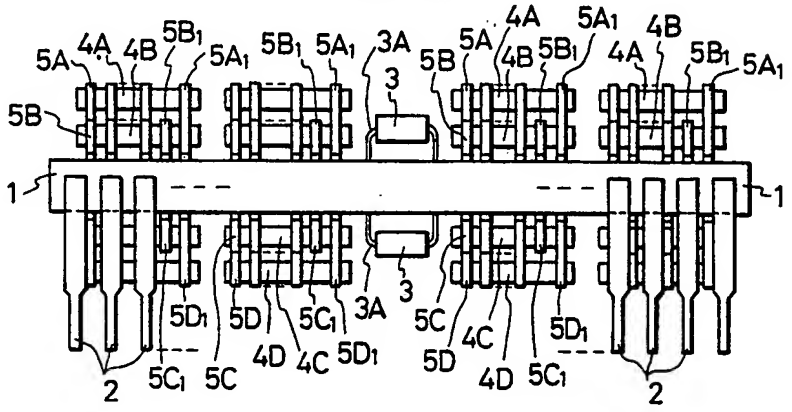
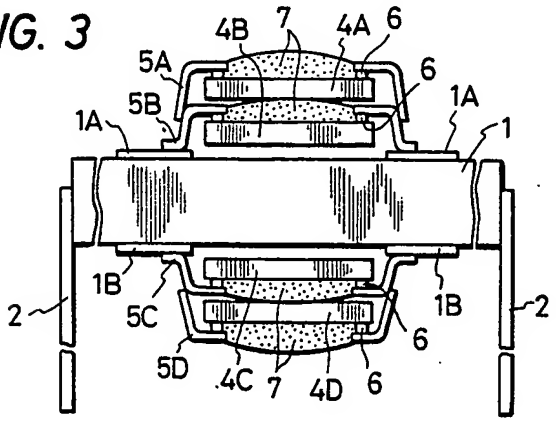


FIG. 3



The specification describes the module base plate as a "mounting base plate." (Watanabe, col. 1, ll. 17-18). Figure 2 shows 16 individual semiconductor chips mounted in four 2-high stacks on both sides of module base plate 1. An alternative embodiment mounts the chips in 3-high stacks on the module base plate 1. (Watanabe, col. 6, ll. 53-68; Fig. 4).

The Watanabe specification describes this module base plate 1 as made of laminated ceramic: "Referring to FIGS. 1 thru 3, numeral 1 designates a module base plate, which is constructed by stacking pluralities of ceramic layers and wiring layers by the use of laminated

ceramic." (Watanabe, Col. 5, ll. 38-41).

There is "wiring" within module base plate 1: The individual leads 5B and 5C of semiconductor chips 4B and 4C "are connected to a decoder 3 and leads 2 through wiring (not shown) within the module base plate 1." (Watanabe, col. 5, ll. 66-68, col. 7, ll. 14-17).

b) How the Rejections Erroneously Read Claim 1 On The Module Base Plate 1 of Watanabe.

The Rejection contends that the "flex substrate" limitation in claim 1 is met by the module base plate 1 of Watanabe. The March Rejection states: "Watanabe (Figures 1 & 2) teaches a chip stack comprising: a flex circuit comprising: a flex substrate [1]; ..." (March Rejection, at p. 3). The March Rejection continues:

> Watanabe teaches that the flex substrate is made of a ceramic (5, 38+), which is flexible to at least some degree. The specification does not define what flexible means. There is no quantification for the term flexible, therefore **a ceramic material meets the limitation of the claims because all things are flexible, at least to some degree."** (March Rejection, at p. 3) (emphasis supplied).

The October Rejection amplifies this reasoning: "It is the examiner's position that the metes and bounds of the word flexible is not defined in the specification, therefore the word is given its broadest reasonable meaning. **The examiner asserts all substrates are flexible, under the proper conditions. Any substrate can be made to bend.** Therefore, the flexible limitation has been met by Watanabe." (October Rejection, at pp. 2, 4) (emphasis supplied).

c) Nothing In Watanabe Teaches Directly or Indirectly That The Module Base Plate Is A Flexible Substrate.

The 102(b) rejection is invalid because the module base plate 1 of Watanabe does not satisfy the limitation of a "flex substrate." The module base plate 1 of Watanabe was held to satisfy the limitation of a "flex substrate" because the "metes and bounds of the word 'flexible' is not defined in the specification, therefore the word is given its broadest reasonable meaning"; and "all substrates are flexible, under the proper conditions." (October Rejection, at p. 2. *See also* October Rejection, at p. 4; March Rejection, at p. 3).

It is true that the word "flexible" is not defined in the specification. Indeed, the word "flexible" does not appear anywhere in the specification or in claims 1-9. Claims 1-9 include limitations directed to a "flex" substrate (and a "flex" circuit) but do not otherwise use the word

"flexible." Similarly, although the specification describes structure corresponding to a "flex substrate" 14 (Specification, par. 0016), the word "flexible" does not appear in the specification.

It was the Examiner, in the March Rejection, who first used the word "flexible" in connection with the "flex substrate" limitation (March Rejection, at p. 3; October Rejection, at pp. 2, 4). It is unclear whether it is the Examiner's position that (i) "flexibility" is inherent in the meaning of a "flex substrate," so that the "flex substrate" recited in claim 1 is construed to be necessarily flexible, or (ii) a "flex substrate" is exactly synonymous with a "substrate" that flexes or is flexible. For the purposes of this appeal, however, it is not necessary to take a position one way or the other on the Examiner's claim construction. Because Watanabe does not describe a flexible "flex substrate" or a substrate that flexes or is flexible, the 102(b) rejection based on Watanabe cannot stand.

In other words, assuming *arguendo* that the "flex substrate" limitation requires flexibility, the rejection nonetheless fails. The scope of a claim is determined "not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction 'in light of the specification as it would be interpreted by one of ordinary skill in the art.'" *Phillips v. AWH Corporation*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (*quoting In re American Academy of Sci-Tech Ctr,* 367 F.3d. 1359, 1364 (Fed. Cir. 2004). The module base plate 1 of Watanabe cannot be *reasonably* construed as a flex substrate that flexes, or a flexible substrate, satisfying the "flex substrate" limitation of claim 1, for at least the following reasons.

First, nowhere in Watanabe is the module base plate 1 identified or described as a "substrate," a "flex substrate," or a "flexible substrate."

Second, nowhere does Watanabe express or imply that the module base plate 1 is flexible, bendable, elastic, pliant, supple, springy, resilient, not rigid, not stiff, or any other reasonable synonym of flexible.

Indeed, Staktek respectfully submits that longitudinal and transverse structural *rigidity* is inherent in both the mode of manufacture (ceramic laminate) of the module base plate 1 and its intended use as a leaded mounting plate for longitudinally-dispersed stacks of leaded chips. (Watanabe, Figs. 2, 3). No other structure in Watanabe provides the structural integrity required to support the linearly-dispersed collection of stacked memory chips shown in Figures 2 and 3 of Watanabe. The module base plate 1 in Watanabe, in other words, must be inherently rigid - not flexible.

Finally, assuming *arguendo* that the module base plate 1 is a "substrate," it is *not* the case that "all substrates are flexible," so as to satisfy the limitation of a flex substrate, as suggested in the Rejection. (October Rejection, at pp. 2, 4). The Federal Circuit recently reaffirmed in its *en banc* opinion in *Phillips v. AWH Corporation* that the "claims themselves provide substantial guidance as to the meaning of particular claim terms [and the] context in which a term is used in the asserted claim can be highly instructive." *Phillips v. AWH Corporation*, 415 F.3d 1303, 1314 (citations omitted). "To take a simple example," the court continued, "the claim in this case refers to "steel baffles," which strongly implies that the term "baffles" does not inherently mean objects made of steel." *Id.*

Here, the use of the compound phrase "flex substrate" in claim 1 strongly implies that the term "substrate" as used in the limitation (flex substrate in claim 1) does not inherently mean flexibility. *See Phillips v. AWH Corporation*, 415 F.3d at 1314 (use of "steel baffles" in claim implies that not all baffles are steel). Even if the module base plate 1 is taken to be a "substrate," as implicitly assumed by the Rejection, it cannot be assumed to be a *flex* substrate (or *flexible* substrate). As noted above, there is no other teaching in Watanabe to show that the module base plate 1 flexes or is flexible.

In short, Watanabe does not disclose the "flex substrate" limitation of claim 1, and hence does not anticipate claim 1 under 35 U.S.C. § 102(b).

2. Watanabe Does Not Disclose "Integrated Circuit Chip Packages."

Alternatively, Watanabe does not anticipate claim 1 for the independent reason that Watanabe teaches no structure that satisfies the "integrated circuit chip package" limitation of claim 1. Watanabe teaches the stacking of semiconductor chips. (*See, e.g.,* Watanabe, Cols. 1, ll. 10-19, Col. 18, ll. 11, 35). Watanabe repeatedly emphasizes, however, that the semiconductor chips are *not* sealed within packages:

- "Each of the semiconductor chips 4A, 4B, 4C, and 4D has, for example, a static RAM constructed therein. Structurally, *it is not sealed with a package made of ceramic, a resin or the like*, but its surface provided with semiconductor elements and wiring is molded with a resin 7." (Watanabe, Col. 5, ll. 43-48) (emphasis supplied).

- "[T]the semiconductor chips are *not sealed with in packages*, therefore the packaging density of the semiconductor chips on the module base plate can be increased." (Watanabe, Col. 2, ll. 37-40) (emphasis supplied).

- "As described above, the semiconductor device is constructed by installing on the module base plate 1 the respective semiconductor chips 4A, 4B, 4C and 4D to which the corresponding leads 5A, 5B, 5C and 5D are connected by the TAB *without encapsulation in packages*, whereby the area which the single semiconductor chip 4A, 4B, 4C or 4D occupies on the module base plate 1 can be reduced, and hence, the larger number of semiconductor chips 4A, 4B, 4C and 4D can be installed on the module base plate 1. That is, the packaging density of the semiconductor device can be heightened." (Watanabe, Col. 6, ll. 33-43) (emphasis supplied)

Because Watanabe disclaims use of integrated circuit chip *packages*, it does not satisfy the "integrated circuit chip packages" limitation of claim 1. Claim 1 therefore is not anticipated by Watanabe.

3. Conclusion Regarding 102(b) Rejection.

In summary, Watanabe neither describes nor suggests the flex substrate or the integrated circuit chip packages limitations of claim 1, and thus does not anticipate claim 1. *See, e.g., Verdegaal Bros.*, 814 F.2d at 631, 2 USPQ2d at 1053. Claims 2, 3, 4, 6, and 7, which depend directly or indirectly from claim 1, are not anticipated by Watanabe for the reasons detailed above with respect to claim 1. See 35 U.S.C. § 112, ¶ 4. Staktek respectfully requests that the Board reverse the Examiner's rejection of claims 1-4, 6 and 7.

B. Rejection of Claims 5, 8 and 9 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Watanabe

Dependent claims 5, 8, and 9 stand rejected under 35 U.S.C. § 103(a) as obvious over Watanabe. (March Rejection, at pp. 5-7; October Rejection at pp. 3, 6-8). The rejection is improper and should be reversed because the Rejection does not make a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references) must teach or suggest *all* the claim limitations. MPEP § 2143; *see, e.g., In re Royka*, 490 F.2d 981, 985 (CCPA 1974) (holding that establishing prima facie obviousness requires that all the claim limitations must be taught or suggested by the prior art).

For the reasons described above, Watanabe does not teach or suggest the "flex substrate" and "integrated circuit chip packages" limitations of claim 1. Claims 5, 8, and 9 depend, directly or indirectly, from claim 1, and thus include all limitations of claim 1. Consequently Watanabe does not teach or suggest all limitations of claims 5, 8, and 9, and claims 5, 8, and 9 are not obvious over Watanabe. *See, e.g., Verdegaal Bros.*, 814 F.2d at 631, 2 USPQ2d at 1053.

Further, to establish a *prima facie* case of obviousness, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; there must be a reasonable expectation of success; and the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP § 2143; *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 5, 8, and 9 are not obvious over Watanabe because each depends, directly or indirectly, from claim 1, and hence each includes the "integrated circuit chip packages" limitation of claim 1. Watanabe, however, teaches *away* from the use of integrated circuit chip packages. Watanabe teaches use of a separate structure (the ceramic base plate) to supply the structural integrity needed for a device to perform as a module. In contrast, the present invention obtains its structural integrity from the packaging of the devices from which its module is constituted. This is a clear distinction between the respective strategies for building a circuit module. Thus, because Watanabe provides a ceramic base to provide structure for unpackaged die, it could not and does not suggest (a) using a flexible connector rather than a rigid base plate or (b) the use of packaged devices rather than die. Such an approach is that of the present invention and is actually taught away from by Watanabe .

At Col. 2, ll. 37-41, the reason for the Watanabe use of unpackaged circuits is explained, "*the semiconductor chips are not sealed with in packages, therefore the packaging density of the semiconductor chips on the module base plate can be increased.*" (emphasis supplied). For Watanabe, there is a reason to use unpackaged chips. Density can be increased. Thus, Watanabe teaches away from use of the packaged devices. On the other hand, the present invention employs packaged devices to provide structure for the module. In Watanabe, that structural integrity is provided by the ceramic base plate. Thus, Watanabe gets structural integrity from the connector and not the integrated circuit devices while in the present invention, structure is provided by the devices and not the connector. These different perspectives on solving the issues of structure are mutually exclusive.

In summary, the independent claims from which claims 5, 8, and 9 depend are not obvious over Watanabe because Watanabe teaches away from the "integrated circuit chip packages" limitation. If an independent claim is nonobvious under 35 U.S.C. 103, then any

claim depending therefrom is nonobvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Claims 5, 8, and 9 therefore are nonobvious, and Staktek respectfully requests that the Board reverse the Examiner's rejection of claims 5, 8, and 9.

CONCLUSION

For the foregoing reasons, Staktek respectfully submits that claims 1-9 are patentable over Watanabe. Accordingly, Staktek respectfully requests that the rejections of claims 1-9 be reversed.

Respectfully submitted,

Date: March 17, 2006

By: _____

J. Roger Williams, Jr.
Reg. No. 45,428

Andrews Kurth LLP
111 Congress Avenue
Suite 1700
Austin, Texas 78701
Telephone: (512) 320-9200
Facsimile: (512) 320-9292

VIII. CLAIMS APPENDIX

1. (Original) A chip stack comprising:

a flex circuit comprising:

a flex substrate;

a first conductive pattern disposed on the flex substrate; and

a plurality of leads extending from the flex substrate and electrically connected to the first conductive pattern;

at least two integrated circuit chip packages electrically connected to the first conductive pattern.

2. (Original) The chip stack of Claim 1 wherein:

the flex substrate defines opposed top and bottom surfaces; and

the first conductive pattern comprises:

a first set of flex pads disposed on the top surface of the flex substrate; and

a second set of flex pads disposed on the bottom surface of the flex substrate;

the flex pads of the first and second sets being electrically connected to the leads, with one of the integrated circuit chip packages being disposed upon the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set and one of the integrated circuit chips being disposed upon the bottom surface of the flex substrate and electrically connected to at least some of the flex pads of the second set.

3. (Original) The chip stack of Claim 2 wherein the flex pads of the first and second sets are arranged in identical patterns.

4. (Original) The chip stack of Claim 2 wherein:

the flex substrate has a generally rectangular configuration defining opposed pairs of longitudinal and lateral peripheral edge segments; and

the leads extend from at least one of the longitudinal and lateral peripheral edge segments of the flex substrate.

5. (Original) The chip stack of Claim 1 wherein each of the leads is an S-lead.
6. (Original) The chip stack of Claim 2 wherein the integrated circuit chip packages each comprise:

    a package body having opposed, generally planar top and bottom surfaces; and

    a plurality of conductive contacts disposed on the bottom surface of the package body;

    the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the first set, with the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the second set.
7. (Original) The chip stack of Claim 6 wherein the flex pads of the first and second sets and the conductive contacts are arranged in identical patterns.
8. (Original) The chip stack of Claim 6 wherein each of the integrated circuit chip packages comprises a CSP device.
9. (Original) The chip stack of Claim 8 wherein the integrated circuit chip packages are each selected from the group consisting of:

    a BGA device;

    a fine pitch BGA device; and

    a flip chip device.

IX. EVIDENCE APPENDIX

No evidence is submitted.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings in which a decision has been rendered by a court or the Board.